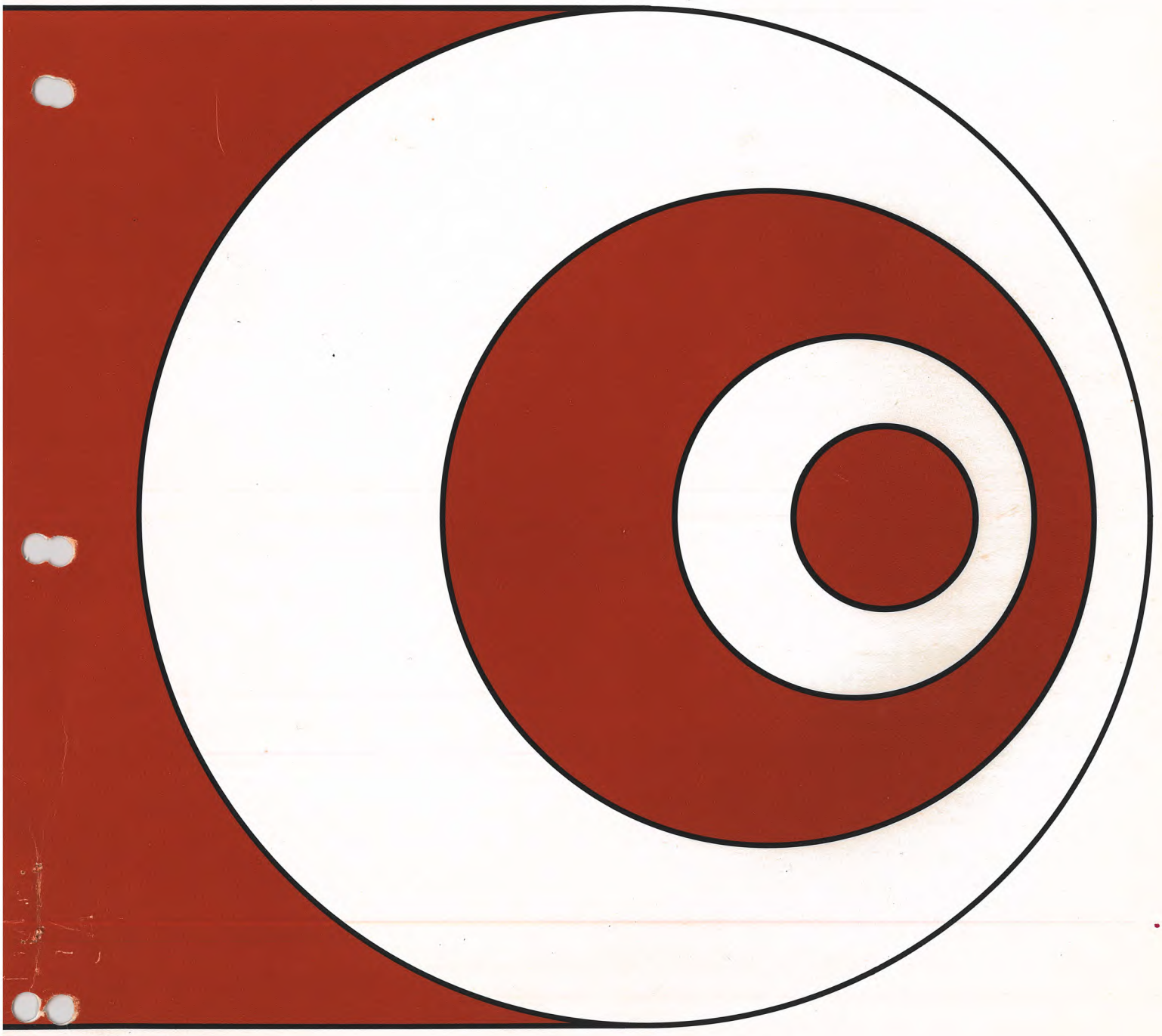
SIGNETICS TWIN

HIGH SPEED

MASTER/SLAVE MEMORY

SUPPLEMENT TO REFERENCE MANUAL



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HIGH SPEED

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SUPPLEMENT TO REFERENCE MANUAL

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Signetics Part Number: TW 140 000 012

TABLE OF CONTENTS

1.0 PRODUCT OVERVIEW

1.1 The 80K Memory Card has been developed to:

1. replace the TWIN multiboard memory with a one board memory system which can supply all TWIN memory requirements.
2. speed up the TWIN memory system access time to reduce the number of wait-states, providing for real-time emulation of the faster CPU versions.

1.2 The 80K Memory Card contains up to 80K bytes of dynamic RAM and 256 bytes of boot PROM. The memory card uses Signetics 2690 16K x 1 memory chips configured as an array of 80K bytes.

1.3 The 80K Memory Card provides random access storage for programs and data that execute on the TWIN Development System.

1.4 This memory card must reside on the master side of the TWIN card cage. All RAM locations must be written at power on to initialize the parity bits.

1.5 Typical applications for the 80K Memory Card are:

1. Memory system for the TWIN
2. Memory module for any byte oriented microprocessor which requires 80K bytes or less of RAM.

2.0 USER REQUIREMENTS

2.1 PRODUCT FEATURES

1. Internal parity generation and detection
2. Hidden Refresh
3. 256 byte boot PROM using the Signetics 82S141 512 x 8 PROM.
4 400 ns access time
5. 900 ns cycle time

2.2 COMPATIBILITY

The 80K Memory Card may be used in any TWIN system to replace the older 4K static memory cards, Slave 4K static TW90012041 and Master Memory/PROM TW 90012161.

2.2.2 Options

This memory card is designed to work with the Signetics 2690-4 16K memory chip. However, 2690-3 memories may be used to upgrade performance if the following timing components are changed:

C2, R35	Sets the time for TRAS
C3	Sets TRAH and a portion of the TRCD delay
C7	Sets the rest of the TRCD delay
C5, R37	Sets the TRA's for refresh operation
C6	Sets TRP

2.2.3 Minimum Configuration

In the minimum configuration the 80K Memory Card has 32K bytes (16K bytes Master and 16K bytes slave). The memory card may be populated in multiples of 16K bytes above the minimum.

3.0 PACKAGING/ENVIRONMENT

The 80K Memory Card system is contained on a single multi-layer printed circuit board.

Size:	11 x 7.4 inches
Weight:	1.0 lbs.
Storage Temp:	-55 to 150 C
Operating Temp:	0 to 70 C

4.0 REFERENCE DOCUMENTATION

TWIN Operator's Guide
TWIN System Reference Manual
TWIN System Maintenance Manual
Signetics TTL Data Book
Signetics Memory Data Book
Signetics 2690 Data Sheet

5.0 HARDWARE DESCRIPTION

5.1 SYSTEM ARCHITECTURE DIAGRAM (See figure 1)

5.2 ELEMENT IDENTIFICATION

The memory is organized into five blocks of 16K bytes. One block is decoded as master memory (16K bytes) and four blocks are decoded as common memory (64 bytes). Each block consists of nine memory chips: Eight for data and one for parity. The memory IC's are Signetics 2690 16K x 1 dynamic memory.

The master memory block is further broken down into a 256 byte boot PROM and 16, 028 bytes of RAM.

The boot PROM occupies master memory address space H'0' through H'FF' and contains the TWIN boot program. When the boot PROM is accessed the RAM-inhibit backplane signal is generated. This signal inhibits access to master memory RAM locations H'0' through H'FF'.

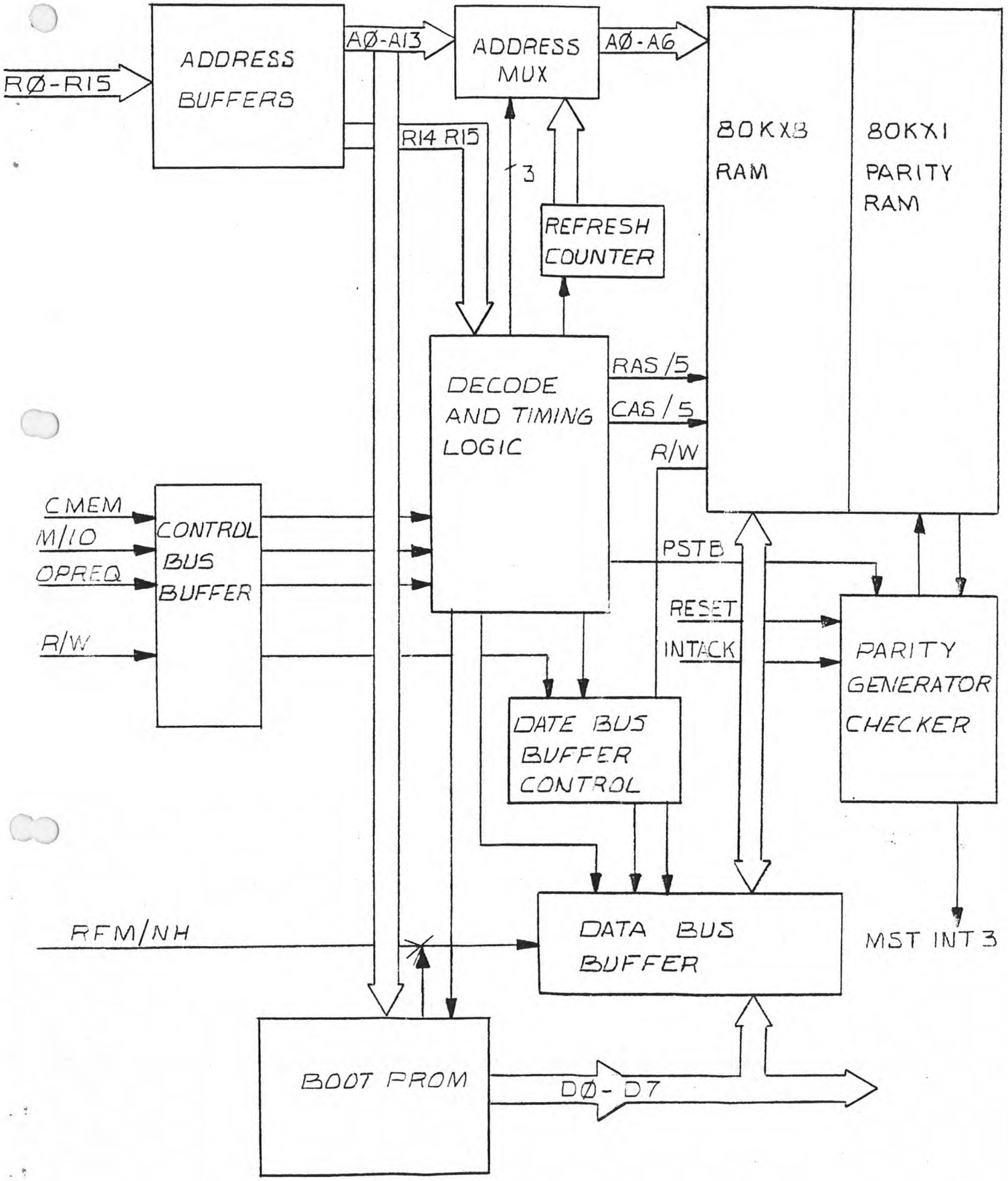

RØ-R15
ADDRESS BUFFERS
AØ-A13
ADDRESS MUX
AØ-A6
80KX8 RAM
80KX1 PARITY RAM
R14 R15
3
REFRESH COUNTER
DECODE AND TIMING LOGIC
RAS/5
CAS/5
R/W
CMEM
M/IO
OPREQ
R/W
CONTROL BUS BUFFER
PSTB
RESET
INTACK
PARITY GENERATOR CHECKER
DATE BUS BUFFER CONTROL
RFM/NH
DATA BUS BUFFER
MST INT 3
BOOT PROM
DØ-D7

FIGURE 1

The parity circuitry generates odd parity every memory WRITE cycle and checks for odd parity every read cycle. If a parity error is detected during a memory read cycle then Master Interrupt 3 is generated. The parity interrupt flip-flop is cleared when Master Interrupt 3 is serviced.

The decode and timing logic generates the strobes and control lines required for memory operation.

5.3 INTERFACE LINES DESCRIPTION

5.3.1 Inputs

All inputs to the 80K memory card are buffered and present a load of 1.8ma or less to the bus. In addition, the address and control bus are terminated with 330 Ohms to +5V and 470 Ohms to ground.

A0 - A15	Address 0 through 15
CMEM	Common or Master Memory
OPREQ	Operation Request
R/W	Read/Write
RESET	System Reset
MST INTACK	Master Interrupt Acknowledge

5.3.2 Outputs

HOLD	Hold (Operation Not Completed)
MSTINT3	Parity Interrupt
I/O	
RAMINH	Inhibit RAM Operations
D0 - D7	Data Bus 0 through 7

5.4 LOGIC DESCRIPTION

This section describes the logical operation of the 80K Memory Card Module. See Memory Card Logic Diagrams.

5.4.1 Selecting the Module

A memory operation begins when the OPREQ (one of eight decoder) becomes true generating one of the signals CB0, CB1, CB2, CB3 or M. When one of these signals go low the decode signal from Pin 8 of A2 goes high. This enables the read/write signal to the memory and data bus buffers and starts the memory access timing chain. (Note: If the RAMINH is true then the memory read/write signal is in the read state and the memory data bus driver is in tri-state).

Memory Access Timing Chain

1. Oneshot A1 Pin 7 is fired by the positive edge of the decode signal for 100 ns. The Pin 7 output sets flip-flop Pin 6 to one and retriggers refresh demand oneshot D1 Pin 7. If refresh is in progress B1 Pin 6 generates the hold signal to the bus for the duration of the refresh cycle.

   If refresh is not in progress the output fires oneshot A1 Pin 10 access oneshot which enables the address MUX to the memory sending the row address to the memory.

2. Oneshot A1 Pin 10 fires for 300 ns. This output latches the selected bank in latch A3 and gates the selected bank through 'NAND' gates at B5 and 'AND' gates at A6 to generate RAS, strobing the row address into the selected bank of 2690 chips.

3. After a short delay caused by inverters F1 Pins 4, 16, 15, 5 and R39, R40 and C3, the ROWEN signal switches the address MUX to send the column address to the memory.

4. After another delay caused by 'NAND' gate E1 Pin 6 and inverter F1 Pin 2, 18 and inverters A4 Pin 2, 18, 11, 9 and R44, R45 and C7, the decode bank is gated through 'NAND' gates B5 and B6 to generate the column address strobe to the selected bank of 2690 chips. If a write operation is in progress the data is loaded into the memory at this time.

5. When the access oneshot A1 Pin 10 times out the read data from the memory is latched into F6 and the access flip-flop B1 Pin 6 is cleared; disabling the address MUX and completing the memory access cycle.

5.4.2 Parity Checking

The falling edge of the access oneshot A1 Pin 18 also generates PSTB. PSTB strobes the parity error flip-flop and if a parity error is detected, then Master Interrupt 3 is generated.

5.4.3 Refresh

The 80K Memory Card performs a refresh cycle at the end of every read or write operation while the OPREQ signal is active true. Therefore, every 128 memory accesses the entire memory is refreshed. If there is no memory access for 12 microseconds the refresh circuitry will force a refresh. When using the 12 microsecond forced refresh mode the entire memory is refreshed every 1.5 milliseconds.

PSTB also fires the refresh oneshot D1 Pin 10 which gates the refresh counter onto the memory address bus. A short delay later (caused by inverter F1 Pins 17, 3, 13, 7, R41, R42, C6) a RAS is generated through 'AND' gate A6 to perform a refresh on all banks of the memory array. After the refresh times out (and a short delay) the count signal increments the refresh counter E5 and E6. Oneshot D1 Pin 7 demands refreshes if no access has been made for 12 us. This oneshot is triggered on every memory access and by the refresh oneshot D1 Pin 10 timing out. When the refresh demand oneshot (D1 Pin 7) times out it will trigger the REFEN oneshot D1 Pin 10. If a memory access is attempted while the refresh oneshot D1 Pin 10 is true the HOLD signal will be generated for the duration of the refresh cycle. At the completion of the refresh cycle, the access oneshot will be fired to complete the memory access requested and the HOLD signal will go false.

5.4.4 Parity Circuitry

The parity circuitry consists of a 74S280 9-bit parity chip (location F7), a parity error flip-flop (location B1 Pin 10), the parity error data input (D2 Pins 1, 2, 3, 4) and the parity error flip-flop reset circuitry (D6, B2 Pins 10, 9, 8). Odd parity is generated by F7 and written into the memory during a write cycle. During memory read cycles, the output of the parity memory is checked by F7 and is strobed into B1 Pin 10. A memory write access or a memory read operation when the RAMINH signal is true will always clear the parity error flip-flop.

5.4.5 PROM Access

The PROM memory is accessed when the master decode of B3 is true and the memory address is between locations H'0' and H'FF. When the PROM is accessed E2 enables the PROM D4. Bus driver D5 also generates the RAMINH signal which blocks the RAM from responding to the access request.

5.4.6 Inhibiting RAM Operations

When RAM-inhibit is active (low), the RAM memory on this card will do a memory read operation but will not place any data on the data bus. To inhibit memory read or write operations the RAM-inhibit signal must be made active within 100 ns of the backplane OPREQ signal becoming active (low).

6.0 MEASURES OF PERFORMANCE

6.1 DIAGNOSTIC AIDS

The jumpers J0 through J5 are permanently installed on the PCB. When cut they may be used to disable various blocks of memory.

J0	Disable master RAM H'0-3FFF
J1	Disable common memory bank 0 H'0-3FFF'
J2	Disable common memory bank 1 H'4000-7FFF'
J3	Disable common memory bank 2 H'8000-BFFF'
J4	Disable common memory bank 3 H'COOO-FFFF'
J5	Disable boot PROM

For example: if a memory card is non-functional; cut J0 and J5 to disable master memory and boot PROM. On a known good memory card cut J1 - J4 to disable common memory. The memory system is now functionally split onto two boards. DIP or a user program running in master can be used to trouble shoot common memory on the other board.

6.2 TESTING THE MEMORY CARD

6.2.1 The 80K memory card is tested using the Diagnostic Interface Program (DIP). The following procedure is used to test the memory card on a TWIN system:

1. Load DIP diagnostic

2. Patch location H'1140 to H'FF(This allows 80K common memory)
   PA1140 cr
   1140=FF....cr

3. To allow 16K patch location H'1140'
   48K H'80'
   64K H'CO'
   80K H'FF'
   (The default value is H'40').

4. Set option 09 (run extended tests; halt on error).
   S009 cr.

5. Load and execute common memory test
   L09010 cr.

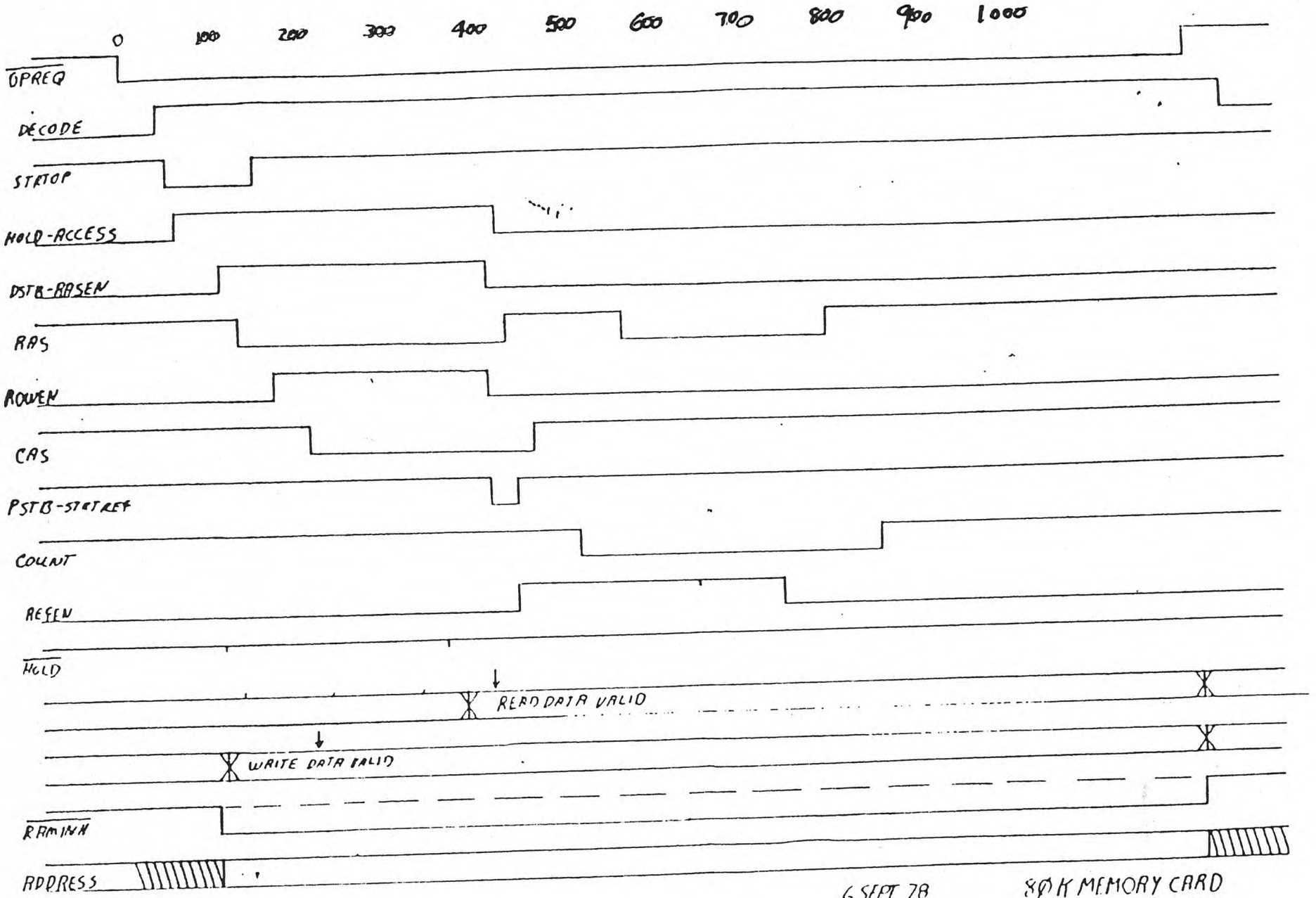
6. Load and execute master memory test
   L09110 cr.

6.2.2 Burn-In

1. Load DIP diagnostic
2. Patch location 1140 to H'FF'
3. Load and execute common and master tests in a loop
   L09

APPENDIX

A) Timing Diagram
B) Pin List
C) Power Requirements
D) Input Loading
E) Output Drive
F) AC Timing



6 SEPT 78
DHW

80K MEMORY CARD
TIMING DIAGRAM

APPENDIX B

PIN LIST FOR 80K MEMORY CARD

PIN	DESCRIPTION	PIN	DESCRIPTION
1-4	+5V Vcc	36	D0
5-10	Not Used	37	D1
11-12	+12V	38	D2
13-14	-12V	39	D3
15-16	Not Used	40	D4
17	A01	41	D5
18	A11	42	D6
19	A21	43	D7
20	A31	44-51	Not Used
21	A41	52	M/IO
22	A51	53	Not Used
23	A61	54	OPREQ
24	A71	55	R/W
25	A81	56	HOLD
26	A91	57-58	Not Used
27	A10	59	RESET
28	A11	60-87	Not Used
29	A12	88	MST INTACK
30	A13	89	MST INT3
31	A14	90-96	Not Used
32	A15	97-100	GND.
33	CMEM		
34	RAMINH		
35	Not Used		

APPENDIX C

POWER REQUIREMENTS

	TYPICAL	MAXIMUM
+5V + -5% (Vcc)	810 mA	1.5 Amps
-12V + -5% (Vbb)	7 mA	50 mA
+12V + -5% (Vdd)	130 mA	200 mA

APPENDIX D

INPUT LOADING

		ONE	ZERO
A0 - A7	I	20 uA	-200 uA
A8 - A13	I	60 uA	-1.8 mA
A14 - A15	I	20 uA	-200 uA
R/W	I	20 uA	-200 uA
CMEM	I	20 uA	-200 uA
M/IO	I	20 uA	-200 uA
OPREQ	I	20 uA	-200 uA
INTACK	I	20 uA	-200 uA
RESET	I	20 uA	-200 uA
RAMINH	I/O	20 uA	-200 uA

The above signals are terminated with 330 Ohm to Vcc and 470 Ohm to Gnd.

DBUS0-DBUS7	I/O	20 uA	-200uA

APPENDIX E

OUTPUT DRIVE -

		ONE	ZERO
MSTINT3	O	4 mA	8 mA
RAMINH	I/O	4 mA	7.8 mA

The above signals are terminated by 330 Ohm to Vcc and 470 Ohm to Gnd.

DBUS0-DBUS7	I/O	-2.6 mA	24 mA
HOLD	O	1 mA	7 mA

APPENDIX F

AC TIMING

Access Time	400 ns
Cycle Time	900 ns
Bus OPREQ to Write	100 ns
Bus OPREQ to RAMINH	100 ns max.

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